Getting Started with the Xilinx Spartan-6 FPGA SP605 Evaluation Kit

UG525 (v1.3) March 29, 2011

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/13/09	1.0	Initial Xilinx release.
12/02/09	1.0.1	Initial release to Web. Minor typographical edits.
06/07/10	1.1	Removed references to ISE software, version 11.1 and 11.3. Removed Figure 1-21 through Figure 1-29, Figure 1-39 through Figure 1-49 and text associated with the figures.
10/15/10	1.2	Updated Figure 1-1, page 8. Revised “Installing the ISE Software,” page 23 describing the use of the software voucher as part of the software registration process.
03/29/11	1.3	Updated Legal DISCLAIMER. Revised Figure 1-1, page 8. Updated website and document links on page 31.

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Appendix A: References

Getting Started with the Spartan-6 FPGA SP605 Evaluation Kit

Introduction

The SP605 Spartan®-6 FPGA Evaluation Kit provides all the basic components for developing broadcast, wireless communications, automotive, and other cost- and power-sensitive applications that require transceiver capabilities in one package. Along with the evaluation board, cables, and documentation, the SP605 evaluation kit provides an integration of hardware, software, intellectual property (IP), and pre-verified reference designs so development can begin right out of the box.

The SP605 evaluation kit provides a flexible environment for system design, including applications that implement features such as high-speed serial transceivers, a PCI Express® interface, DVI, and DDR3 component memory. The SP605 evaluation board includes an industry-standard VITA-57 FPGA Mezzanine Connector (FMC) connector for scaling and customizing to specific applications and markets. Xilinx development tools helps streamline the creation of systems that adhere to complex requirements.

This guide describes how to set up the SP605 evaluation kit and run a diagnostic demonstration that exercises basic board features. It introduces a more complex Base Reference Design (BRD) that exercises key features of the Spartan-6 FPGA. This guide also describes how to install the Xilinx® ISE® Design Suite: Logic Edition software, obtain updates, and generate a license.

SP605 Evaluation Kit Contents

- SP605 Spartan-6 FPGA Evaluation Board
- ISE Design Suite: Logic Edition (device-locked) for the Spartan-6 XC6SLX45T FPGA
  - Includes ChipScope™ Pro software and the ChipScope Pro serial I/O toolkit
  - Includes PlanAhead™ design analysis tool
  - Timing driven place and route, SmartGuide™, and SmartXplorer technology
- Documentation
  - XTP089, *Hardware Setup Guide*
  - UG525, *SP605 Evaluation Kit Getting Started Guide* (this document)
  - UG526, *SP605 Hardware User Guide*
  - UG527, *SP605 Reference Design User Guide*

- Schematics and PCB files
- Universal 12V power supply
- Cables
  - Two USB cables
  - Ethernet
  - DVI-to-VGA adapter
- Reference Designs and Demonstrations
  - SP605 Built-In Self Test Applications Design File
  - SP605 BRD Design Files
  - SP605 MultiBoot Design Files
  - SP605 MIG Design File
  - SP605 GTP IBERT Design Files
  - SP605 PCIe® x1 Gen1 Design Files
- Reference designs, demonstrations, documentation, and applications delivered on USB flash drive to get started quickly

Key Features

Spartan-6 FPGA

- XC6SLX45T-3C in FGG484 package

Configuration

- Onboard JTAG configuration circuitry
- 8 MB Quad SPI flash memory
- 32 MB Parallel (BPI) flash memory
- 2 GB CompactFlash (CF) memory card

Memory

- 128 MB DDR3 component memory
- 32 MB parallel (BPI) flash memory (also available for configuration)
- 8 Kb IIC EEPROM
- 8 MB Quad SPI flash memory (also available for configuration)

Communications and Networking

- 10 Mb/s, 100 Mb/s, 1,000 Mb/s Ethernet
- SFP optical transceiver connector
- GTP transceiver port (TX, RX) with four SMA connectors
- USB To UART bridge
- PCI Express® x1 edge connector

Expansion Connectors

- FMC LPC connector (1 GTP transceiver, 68 single-ended or 34 differential user-defined signals)
- User GPIO with two SMA connectors
- 4 user I/O (1 x 6 header)

Clocking

- 200 MHz oscillator (differential)
- 27 MHz socketed oscillator (single-ended)
- SMA connectors for external clock (differential)
- GTP transceiver reference clock port with two SMA connectors

Display

- Video - DVI/VGA interface
- 16 x 2 LCD character display
- 4 LEDs

Control

- 4 Pushbuttons
- 4 DIP switches

Power

- 12V wall adapter or ATX power supply
- Voltage and current measurement capability of 2.5V, 1.5V, and 1.2V supplies

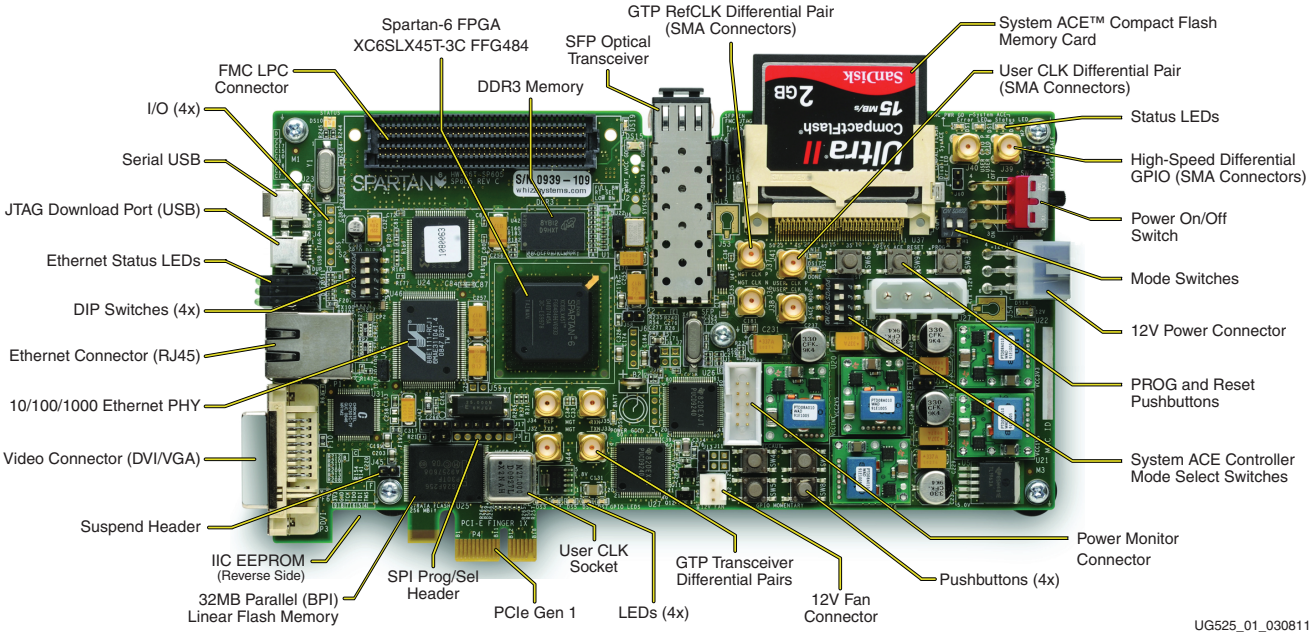

Figure 1-1: **SP605 Evaluation Board Features**

Getting Started with the Base Reference Design Demonstration

Before installing the ISE software, some of the included demonstration designs can be run. These designs are preinstalled on the CompactFlash memory card contained in the SP605 evaluation kit and set up to be run immediately, offering an overview of the board's features. (Additional reference designs and application notes can be downloaded from the Xilinx website.) The default Base Reference Design (BRD) demonstration exercises and/or tests the Ethernet, DVI port, DDR3 memory, DSP, and the overall high-speed logic capabilities of the Spartan-6 FPGA. Figure 1-2 shows a block diagram of the Base Reference Design.

The SP605 BRD demonstration uses the SP605 board to filter images that are transferred via Ethernet between the SP605 board and a PC. This filtered image is then retrieved by the BRD interface GUI and displayed on a PC. A simple loopback test is used to demonstrate the GTP transceivers. A simple memory test demonstrates the DDR3 connectivity using MIG generator in the CORE Generator™ software. Images are sent from a PC via a series of Ethernet packets. This image data is filtered and eventually sent back to the PC for display.

The Ethernet Management section includes an embedded MAC, a GTP transceiver, a PicoBlaze™ host controller, and a Packet Processing Engine. This section provides a way to control various aspects of the demo, transfer images between the SP605 board and a PC, and receive status from the demo. The MAC and packet processing logic can run at 1,000 Mb/s, 100 Mb/s, or 10 Mb/s, depending on the connection speed to the PC.

The Image Processing structure consists of a 5 x 5-pixel 2D FIR filter that is built using the dedicated Spartan-6 FPGA DSP resources. A multiboot feature also allows this design to be implemented using only logic—that is, without the dedicated DSP blocks.

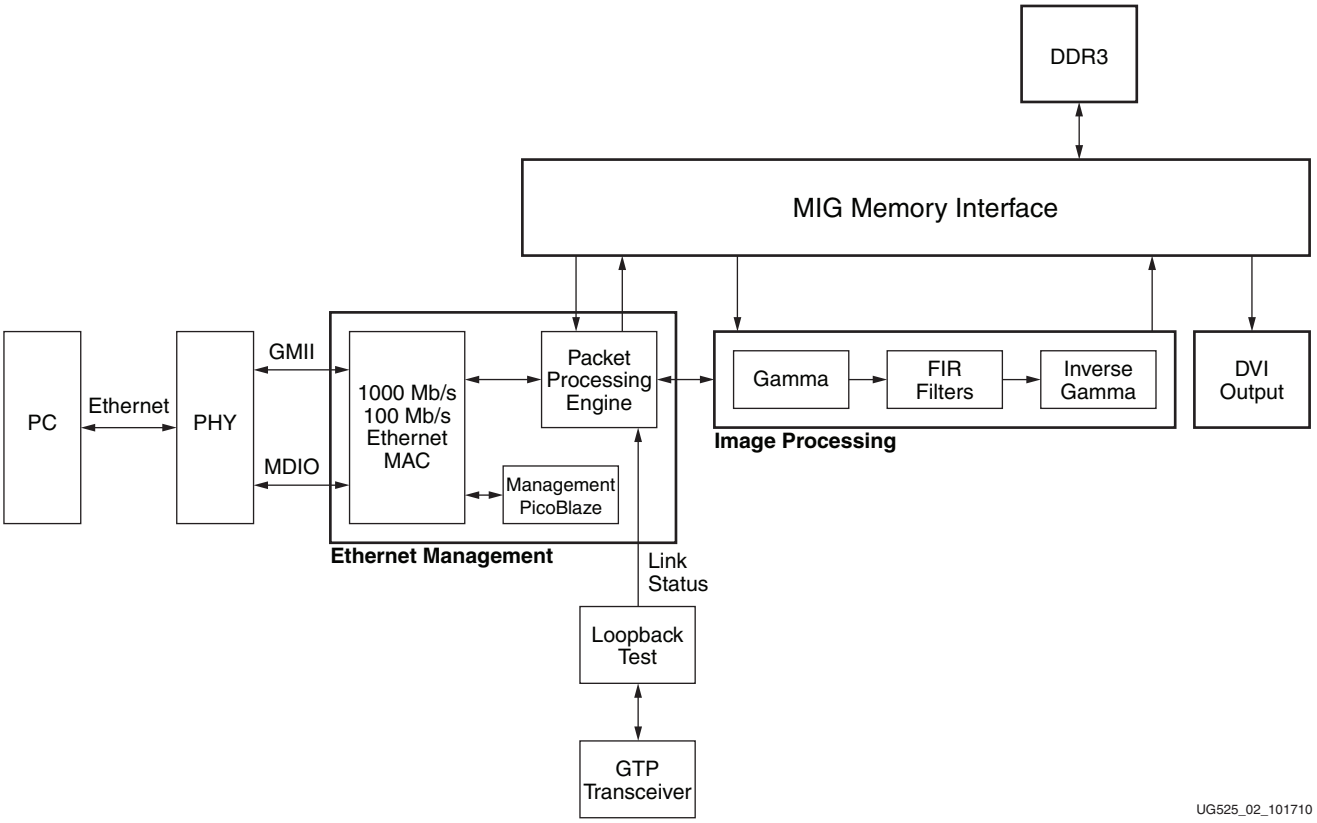

Figure 1-2: **SP605 Base Reference Design Block Diagram**

Setting Up the SP605 Board for the BRD Demonstration

Installing the Application GUI

The Base Reference Design includes an application GUI that must be installed before running the demonstration. On the USB flash drive included with the kit, locate the install image:

`SP605_BRD_Reference Design →SP605_BRD_Application → BaseRefDISetup2_0_5.msi`

This application is used to display the graphical information for the Base Reference Design. Double-click the MSI file to install the software.

Note: The Windows .NET Framework might need to be installed or updated. Go to http://www.microsoft.com/NET/ and click **Get the .NET Framework**.

When running `BaseRefDISetup2_0_5.msi`, an Unknown Publisher Warning appears. Click **Run**, then click **Next** in the Base Reference Design Interface Setup Wizard.

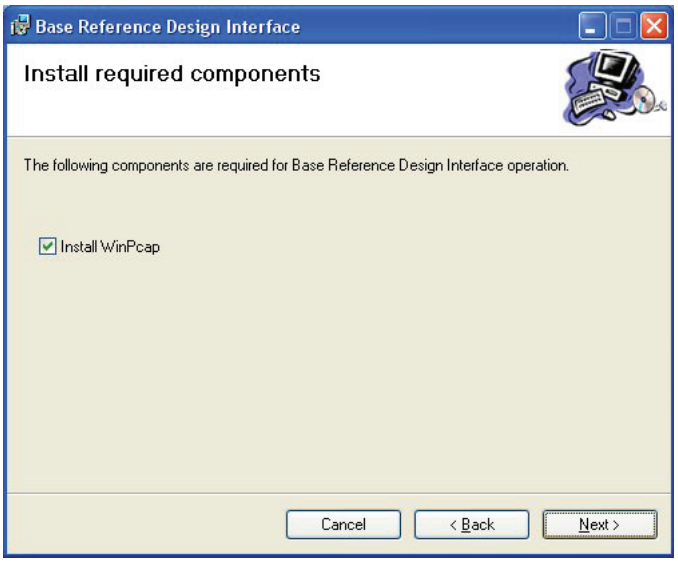

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Figure 1-3: **Base Reference Design Install Window**

This also installs WinPcap, as shown in Figure 1-3 and Figure 1-4. WinPcap is used by the BRD GUI application.

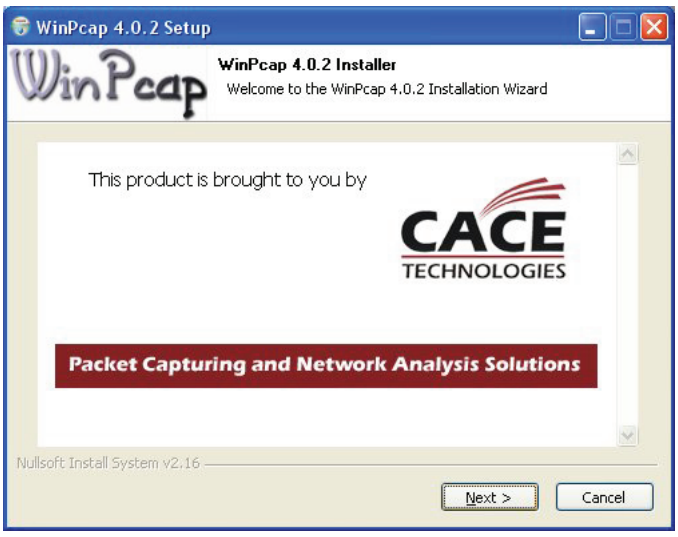

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Figure 1-4: **WinPcap Setup Window**

Default Jumper Settings

As shown in Figure 1-5, 2-pin headers J44 and J46 should have jumpers installed across both pins; 3-pin headers J19 and J22 should have jumpers installed across pins 1–2. Headers J9, J10, J13, J45, J47, J48, J49, J58, and J60 should have no jumpers installed.

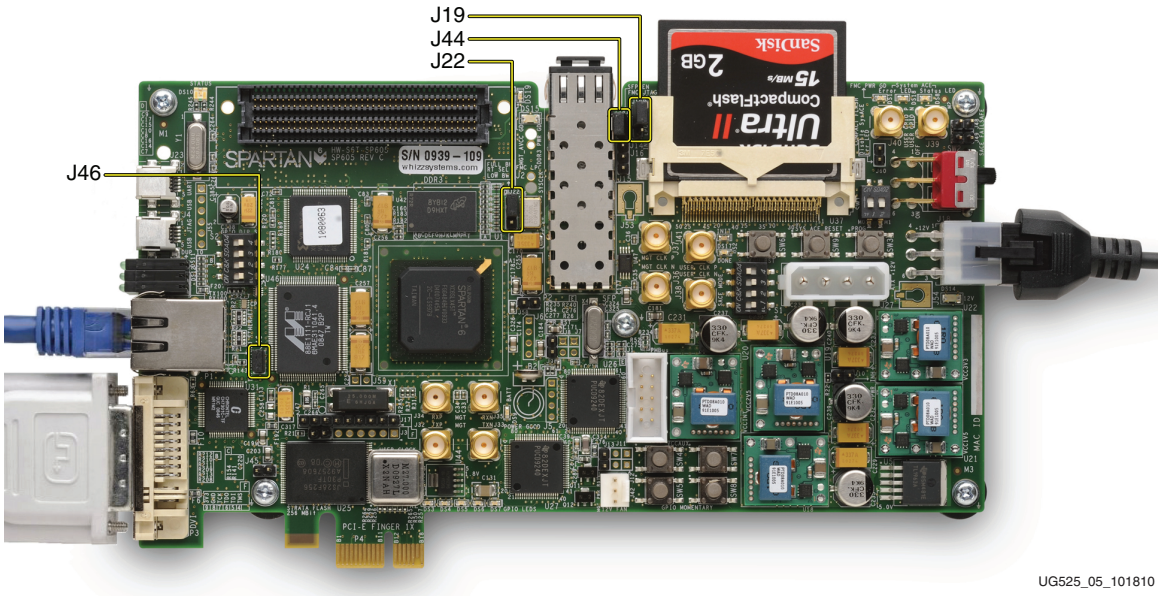

Figure 1-5: **Default Jumper Settings**

Connecting the Cables and CompactFlash Memory Card

The Base Reference Design is one of the demonstrations on the CompactFlash memory card.

Note: Turn off any wireless cards while running this demonstration.

Insert the CF card. Connect the Ethernet cable between the Ethernet RJ45 connectors on the PC and the SP605 board. Connect the DVI port to a DVI-capable monitor, or to a VGA-capable monitor through the DVI-to-VGA adaptor. Plug in the power adaptor to the local AC power. Plug the 12V power jack into the board connector J18. Turn on the power by moving slide switch SW2 to the ON position. See Figure 1-6.

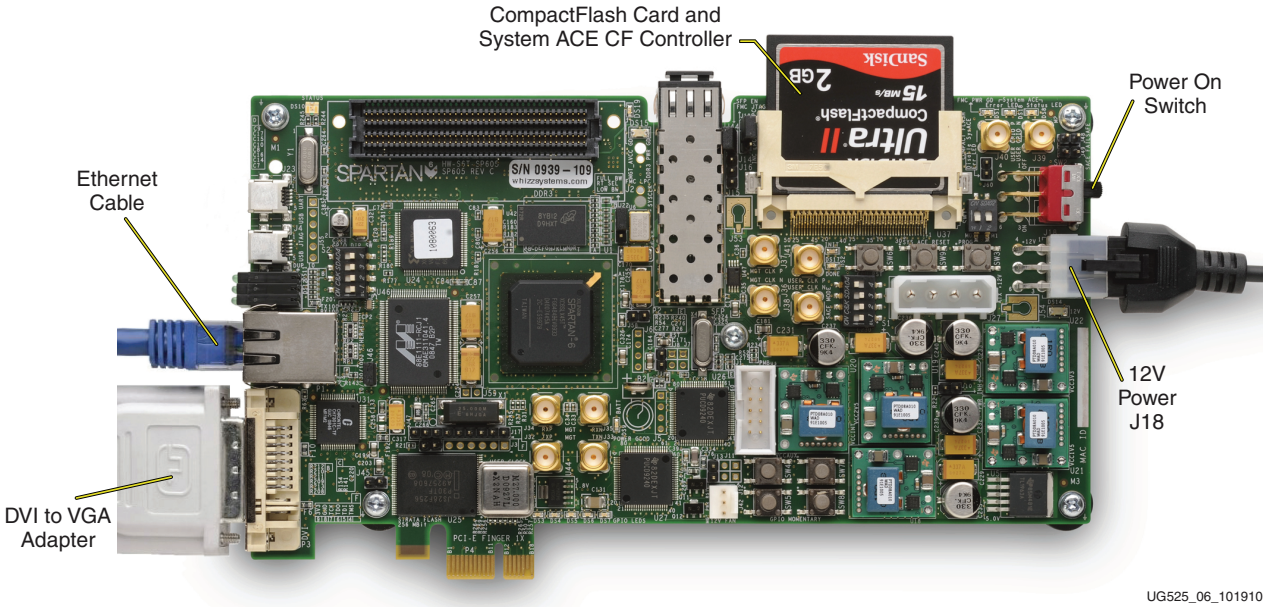

Figure 1-6: **Connecting Cables and CF Card**

Setting the CF Configuration Mode

The Base Reference Design is located in the CompactFlash memory card. To select the CF configuration, set DIP switch (SW1) so that both M0 and M1 are in the OFF position, as shown in Figure 1-7.

Now set the System ACE™ CF Image Select DIP switch (S1) to `1101` where switches 1, 2, and 4 are set to the ON position and switch 3 is set to the OFF position, as shown in Figure 1-7. Setting switch 4 to the ON position enables the System ACE CF controller. Setting switches 1 and 2 to the ON position selects configuration slot 3, where the Base Reference Design demonstration is located.

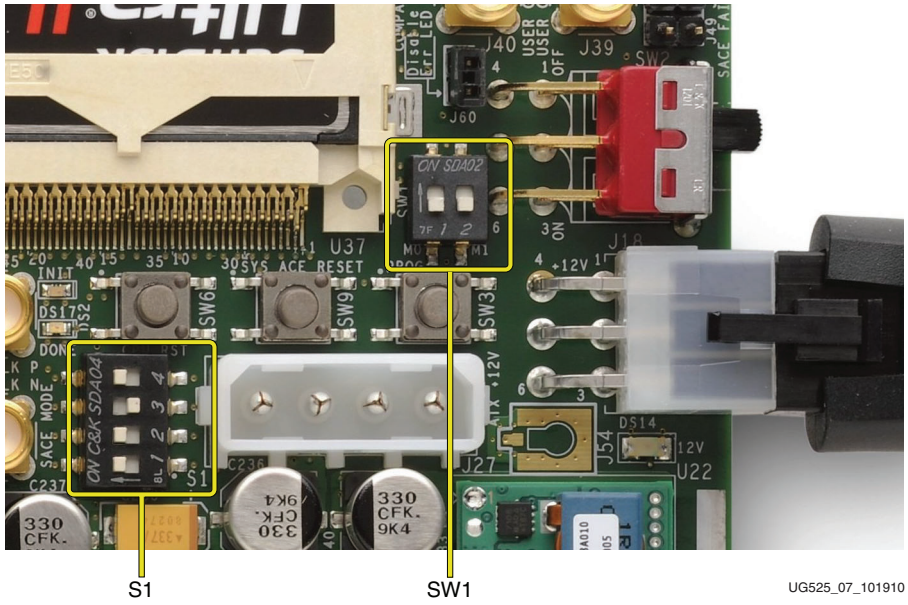

Figure 1-7: **Setting the Mode Select and System ACE CF Select Switches**

Starting the Base Reference Design GUI Application

To start the application GUI, go to the Windows start menu and select **All Programs** → **XILINX** → **Base Reference Design** → **Base Reference Design Interface**

The screen shown in Figure 1-8 is displayed.

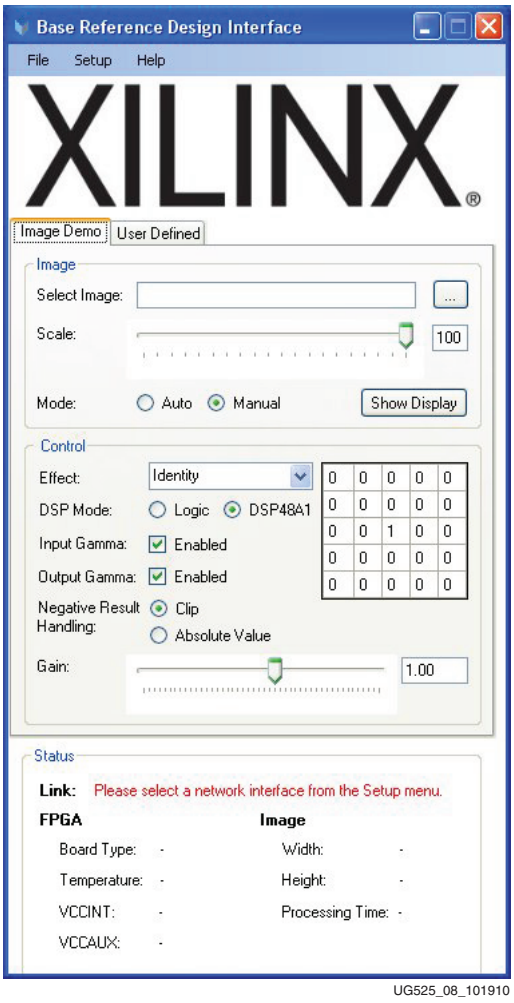

Figure 1-8: **Base Reference Design Interface**

Load the Base Reference Design demonstration from the CompactFlash memory card. To load from the CF card, reset the FPGA by pressing the System ACE CF reset button (SW9), shown in Figure 1-9.

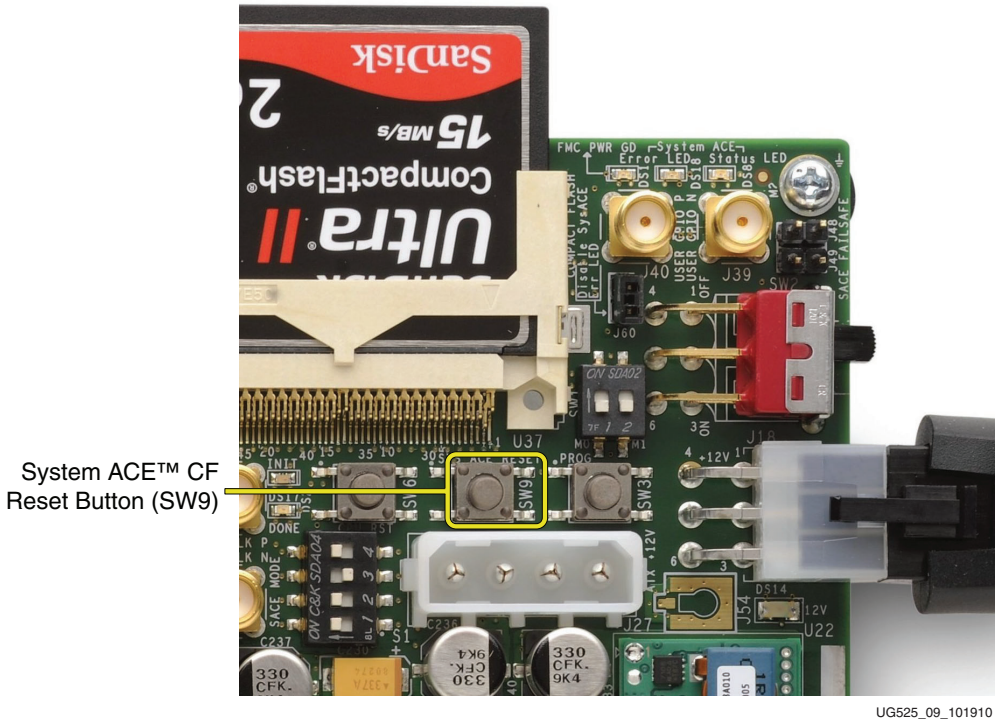

Figure 1-9: **Reset System ACE CF and Load CF Card BRD Demonstration**

Setting Ethernet Link

In the Base Reference Design GUI application, select a network from **Setup** → **Network Interface**, as shown in Figure 1-10. The GUI will indicate *Connected to FPGA* and the Ethernet Status LEDs will be active on the SP605 board.

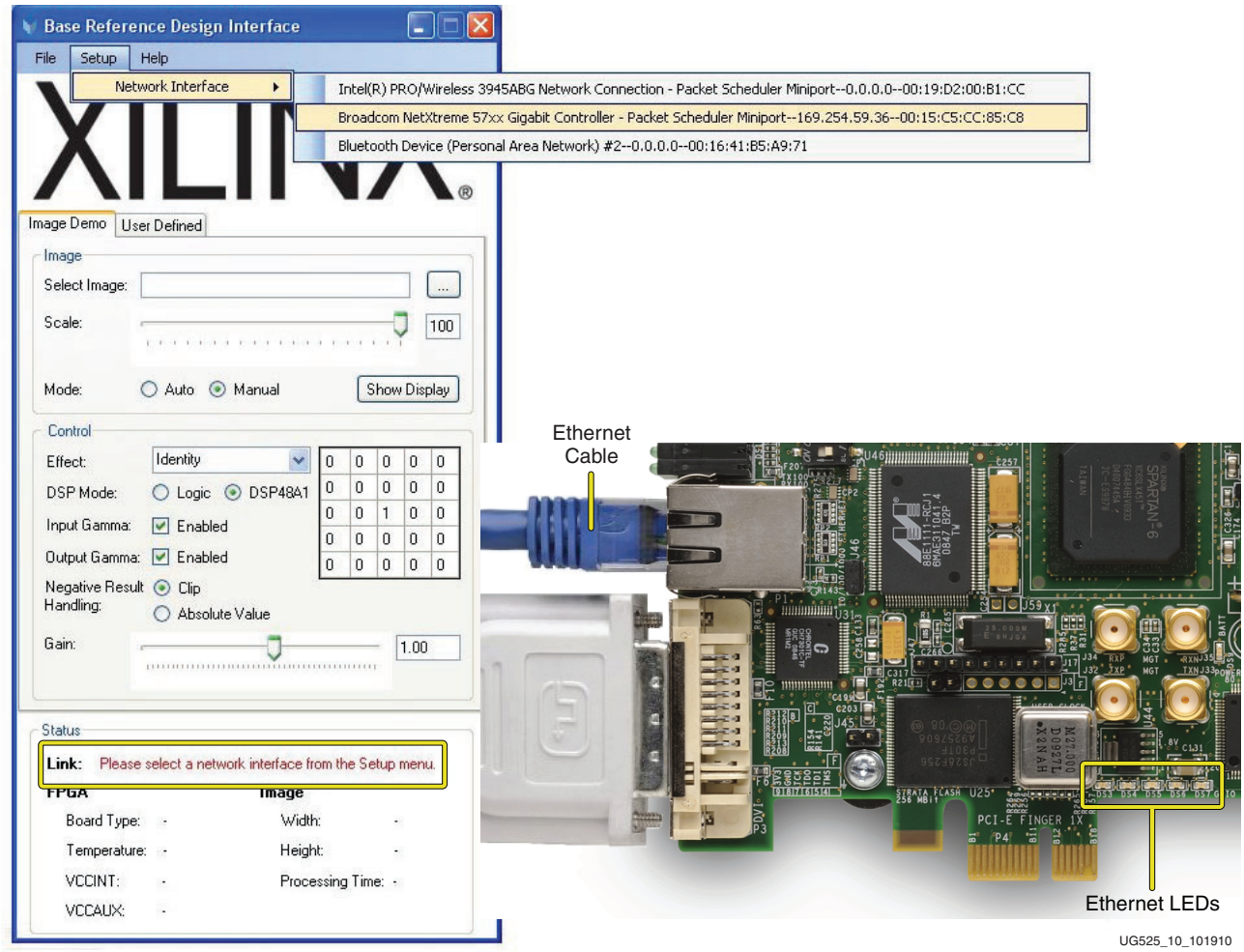

Figure 1-10: **Connecting the Ethernet Link**

Selecting an Image

On the USB flash memory, navigate to the `SP605_BRD_Reference_Design` → `SP605_BRD_Images` directory and select the `fractal1.jpg` image. Then click the **Show Display** button.

The default filter effect is an *Identity* function (Figure 1-11). It takes the loaded image and simply processes it without any filtering effect. The image is sent back over the Ethernet link and displayed in the GUI. It is also sent over the DVI display port.

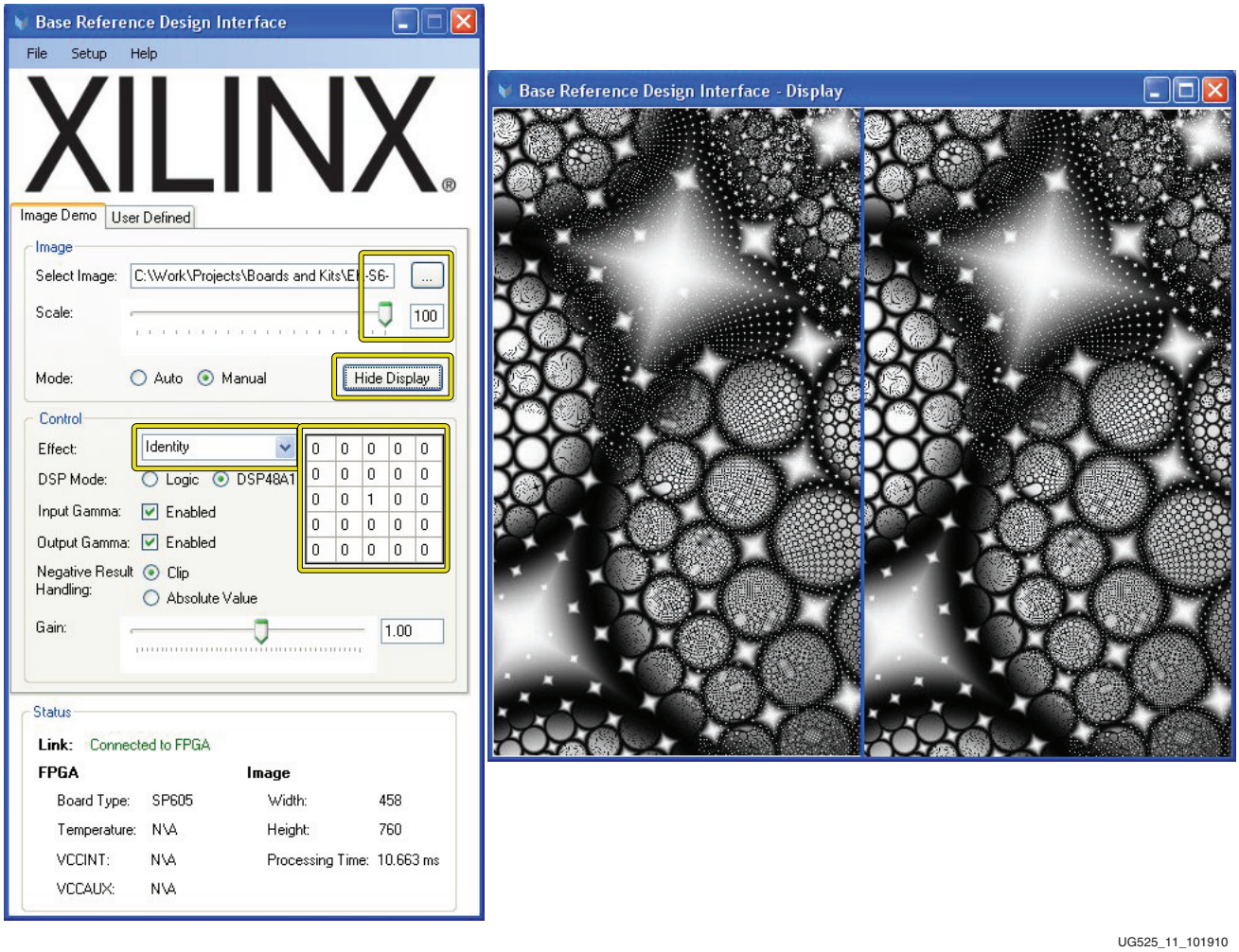

Figure 1-11: **Selecting and Displaying an Image**

Changing the Filter

The default filtering in Figure 1-11, page 16 shows the Identity effect. Now use the Effect drop-down box to select *Edge Detect*. Figure 1-12 shows that the Image is filtered using the transform effect. If a DVI or VGA monitor has been connected, this image will also be displayed on the monitor. Other effects can be selected through interaction with the GUI. Note that the 5 x 5 Filter coefficient table changes every time an effect is changed.

Another feature of this Base Reference Design is MultiBoot. See the DSP Mode radio buttons in Figure 1-12. The two DSP Mode selections are Logic and DSP48A1. The default is DSP48A1, which utilizes the digital signal processing (DSP) element in Spartan-6 FPGAs, the DSP48A1 slice. To demonstrate the performance these DSP48A1 slices provide, notice the processing time for the DSP implementation is around 10.66 ms.

Selecting the Logic DSP mode reloads a new FPGA configuration that only uses FPGA logic resources. When the FPGA is reconfigured, the Program and Done LEDs flash. The Ethernet link also disconnects and then reconnects during reconfiguration. The Logic DSP implementation processes the image at about 5x the DSP48A1 implementation, running at about 53.3 ms.

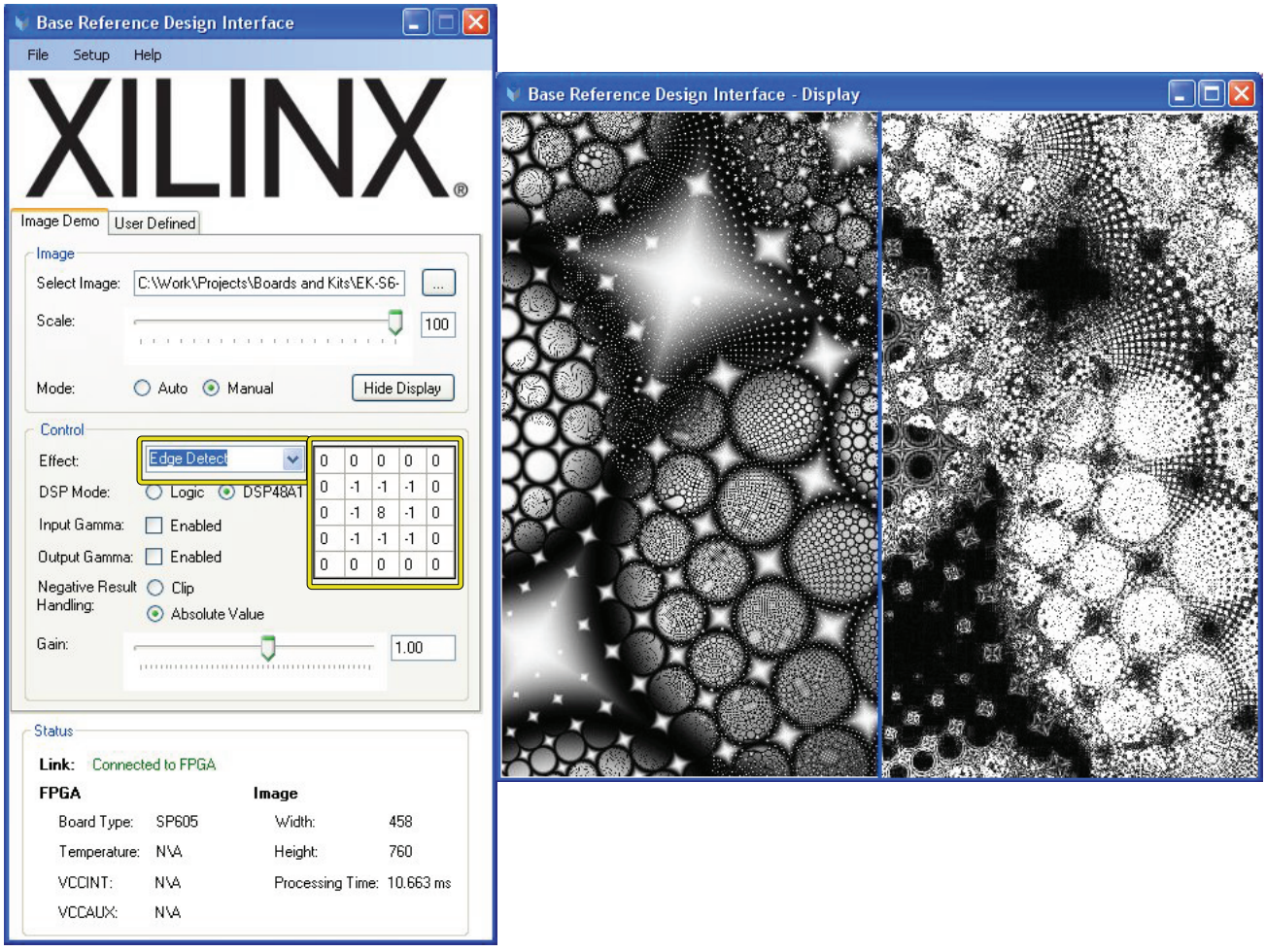

Figure 1-12: **Changing the Filter**

Getting Started with the Diagnostic Flash Demonstration

In addition to the BRD demonstration, a board diagnostic built-in system test (BIST) can also be run that provides an overview of the SP605 board features. The BIST exercises some of the board features, including testing the UART, flashing the LEDs, reading the switches, and testing the Flash memory, DDR3 component memory, IIC bus, Ethernet PHY, and DVI interface.

Setting the Default Jumper Settings

Figure 1-13 highlights the default jumper settings, USB Mini-B JTAG connection, CompactFlash memory card location, and 12V power connection.

As shown in Figure 1-13, 2-pin headers J44 and J46 should have jumpers installed across both pins; 3-pin headers J19 and J22 should have jumpers installed across pins 1–2. Headers J9, J10, J13, J45, J47, J48, J49, J58, and J60 should have no jumpers installed.

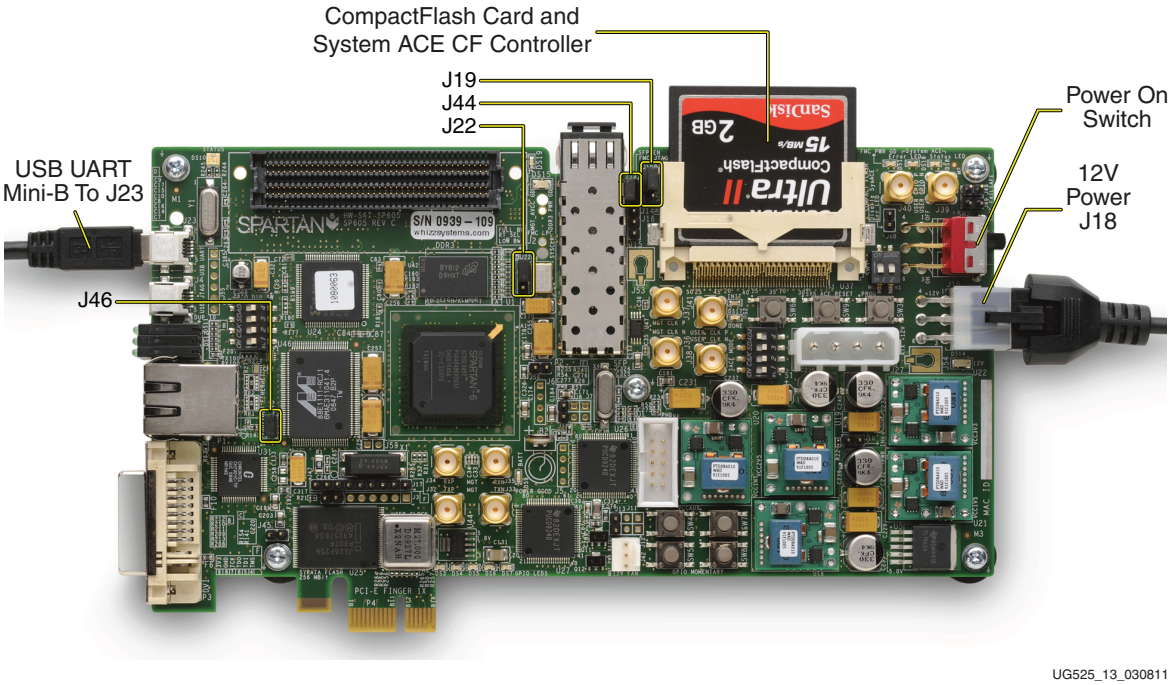

Figure 1-13: **Default Jumper Settings, Cable Connections, and CompactFlash Memory Connection**

Installing CompactFlash Card, USB UART Cable, and 12V Power

1. Install the CompactFlash memory card.
2. Connect the Mini-B USB cable to the USB connector marked J23 (USB UART), and connect the USB A end of the cable to the PC.
3. Plug in the power adapter to local AC power. Plug the 12V power cable into the board connector on J18. Turn on the power by switching the SW1 to the ON position.

Setting the Mode Select and System ACE CF Select Switches

To run the diagnostic demonstration, set the FPGA Mode DIP switch (SW1) to the BPI Configuration Mode, where both M0 and M1 are in the OFF position, as shown in Figure 1-14.

Set the System ACE CompactFlash Image Select DIP switch (S1) to `0001`, where 1, 2, and 3 are set to the OFF position and switch 4 is set to the ON position, as shown in Figure 1-14. This setting addresses configuration 0 on the CompactFlash memory card.

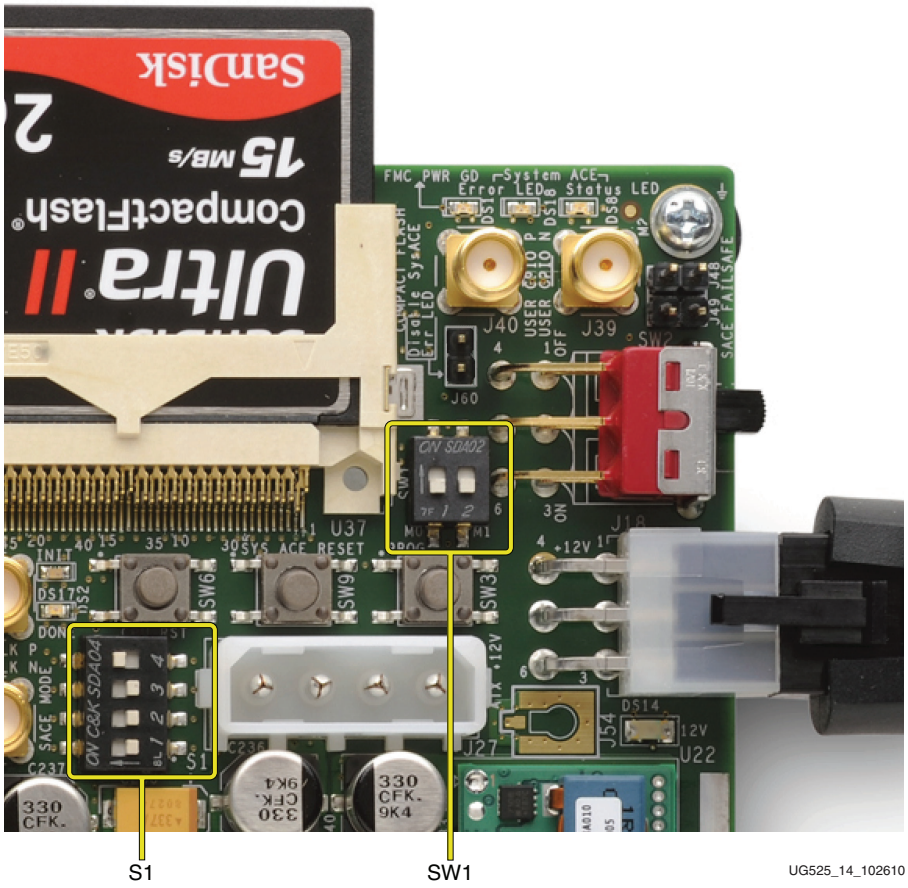

Figure 1-14: **Setting the Mode Select and System ACE Select Switches**

Installing the USB UART Cable and Driver

Make sure the USB Mini-B cable is connected to J23 (USB UART). Install the USB UART driver for the Silicon Labs CP2103GM USB-to-UART Bridge located on the USB drive shipped with the SP605 evaluation kit.

Open the computer's Device Manager dialog box by right-clicking the **My Computer** icon and selecting **Properties**. Select the **Hardware** tab and click the **Device Manager** button. Expand the **Ports** (COM and LPT) entry and see what port the CP210X USB to Bridge Controller is connected to. The example in Figure 1-15 shows the CP210X USB to Bridge Controller connected to COM5, but a customer computer might have assigned this to a different COM Port. Right-click to view additional properties settings.

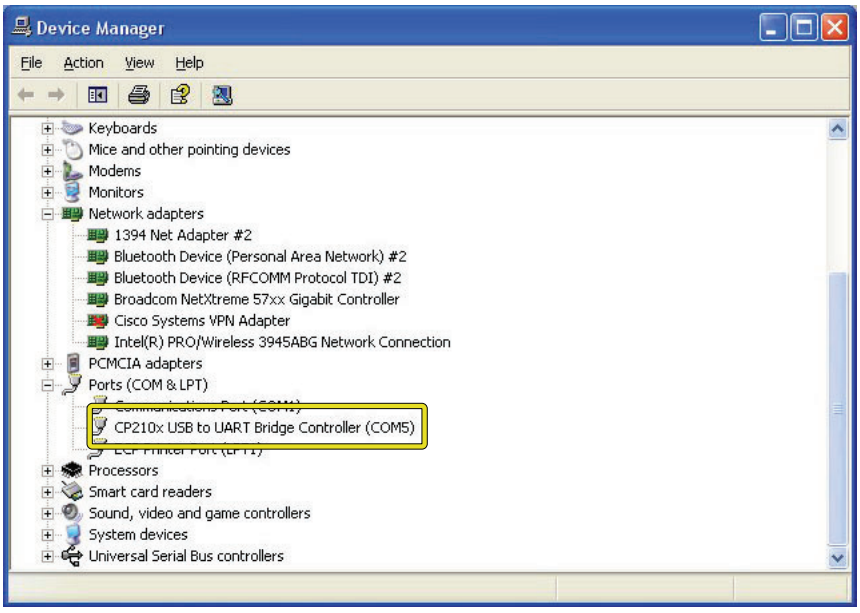

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Figure 1-15: **Setting System Properties to Access USB UART**

Setting Up a Terminal Program

On the PC, open a serial terminal program. This example uses the HyperTerminal serial communications tool included with Windows XP, but any other terminal emulation tool can be used instead.

To open HyperTerminal, select **Start** → **Programs** → **Accessories** → **Communications** →**HyperTerminal**. In the Connection Description window, type `SP605 Board Diagnostic` in the Name box, then click **OK**. See Figure 1-16.

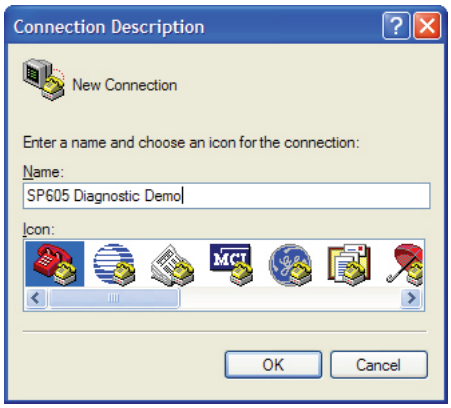

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Figure 1-16: **Opening a Terminal Program**

In the Connect To window, select the **COM port** that the USB cable is connected to — for example, **COM5** — and click **OK**. See Figure 1-17.

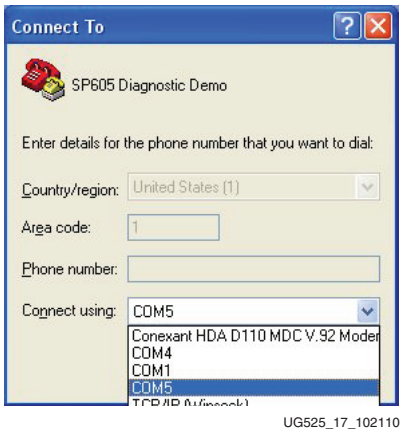

Figure 1-17: **Setting Up a Terminal Program**

Then, in the **HyperTerminal Port Settings** tab, set the following:

- BAUD rate = **9600**
- Data Bits = **8**
- Parity = **None**
- Stop Bits = **1**
- File Control = **None**

Then Click **OK**. See Figure 1-18.

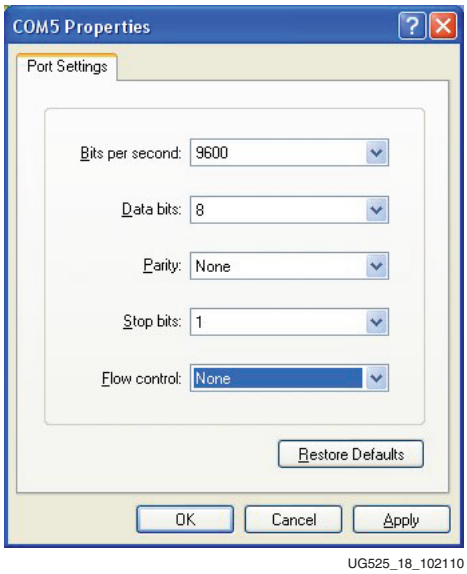

Figure 1-18: **Setting Up the Terminal Program Port**

Configure with BIST Diagnostic Design

Confirm that the System ACE Mode (S1) is set to `0001` and push the System ACE Reset (SW9) shown in Figure 1-19.

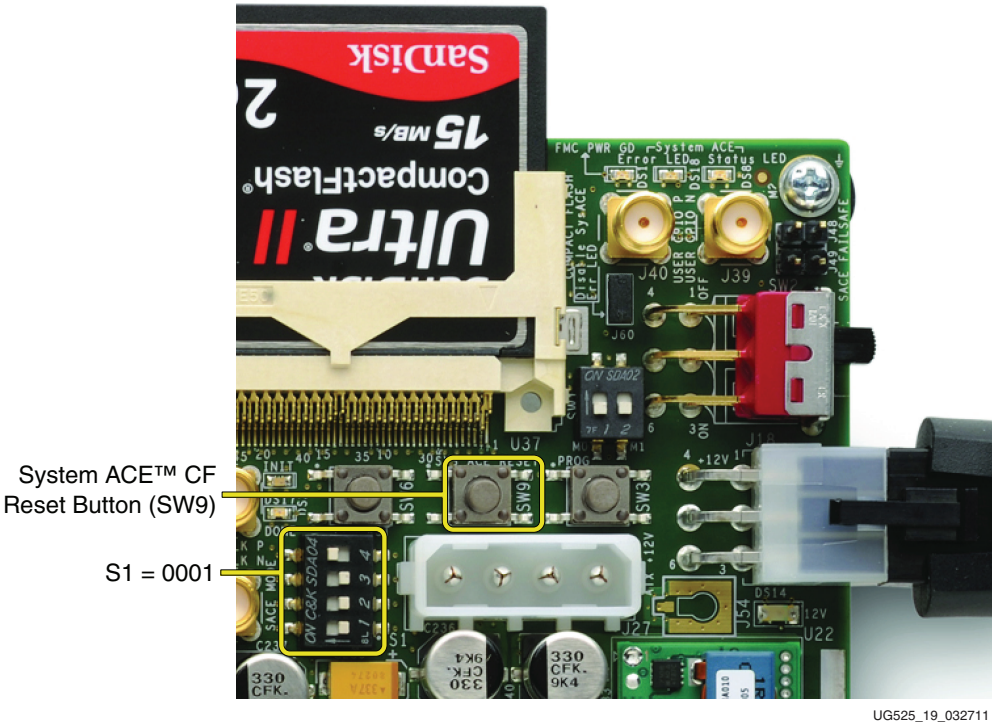

Figure 1-19: **System ACE Reset Switch (SW9)**

Running the Diagnostic Demonstration

From the Diagnostic Demonstration menu, select item 1 **UART Test** to launch a numbers test.

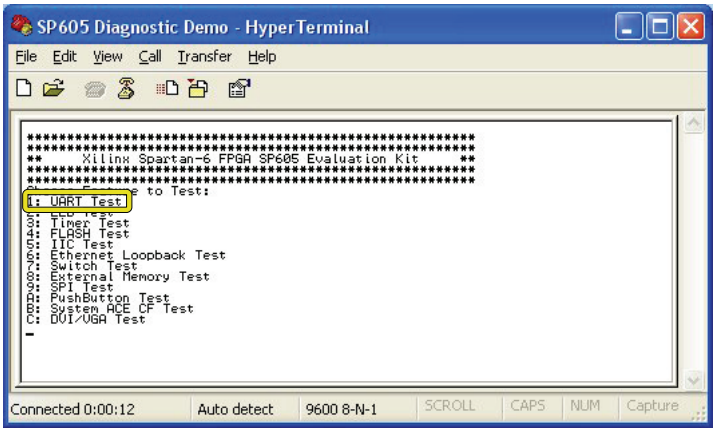

Figure 1-20: **Diagnostic Demonstration Terminal Window Output**

The various diagnostic demonstration menu options can be run to see the different features working on the development board.

At this point, the user should have seen the board powering on, and that features like the UART, switches, LEDs, flash, memories, and ethernet are passing their diagnostic tests. If problems occur, turn to the "Getting Additional Help and Support" section of this guide.

Installing the ISE Software

The SP605 evaluation kit includes entitlement to a seat that permits the ISE Design Suite: Logic Edition to be used with a Spartan-6 XC6SLX45T FPGA. This software can be installed from the DVD provided with the kit. The latest version can also be downloaded from http://www.xilinx.com/support/download/index.htm.

The SP605 evaluation kit also works with the software listed here:

- ISE Design Suite: Embedded Edition
- ISE Design Suite: DSP Edition
- ISE Design Suite: System Edition

Update the software before working with the evaluation kit. Updates can be downloaded from http://www.xilinx.com/support/download/index.htm

To install the ISE Design Suite: Logic Edition software from the DVD included with the SP605 evaluation kit:

1. Activate the software license. See "Redeeming the Software and IP License."
2. Insert the DVD provided with the SP605 evaluation kit in the host computer's drive.
3. Follow the instructions provided by the installation software.

Redeeming the Software and IP License

A software voucher similar to the example shown in Figure 1-21 is included with each SP605 evaluation kit. The voucher contains the code that is used to create a device-locked software license for the ISE software and/or the IP included with the evaluation kit.

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Figure 1-21: **Software Voucher**

To create a license:

1. Go to www.xilinx.com/getlicense/ (Figure 1-22).

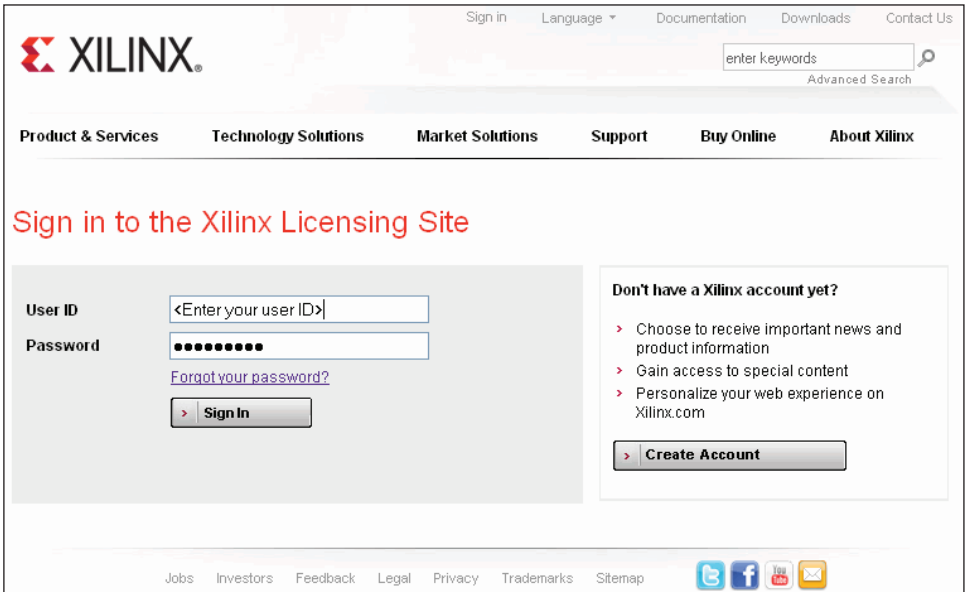


Figure 1-22: **Licensing Site Sign-In Page**

2. To use an existing Xilinx user account, enter **User ID** and **Password** and click **Sign In**. To create a new account, click **Create Account**.

   Note: For questions or other help, contact Xilinx customer service at: http://www.xilinx.com/support/techsup/tappinfo.htm.

3. After signing in, confirm that the contact information is correct and click **Next**.
4. Under the **Create New Licenses** tab, enter the 22-digit code from the voucher in the field shown in Figure 1-23. Click **Redeem Now**.

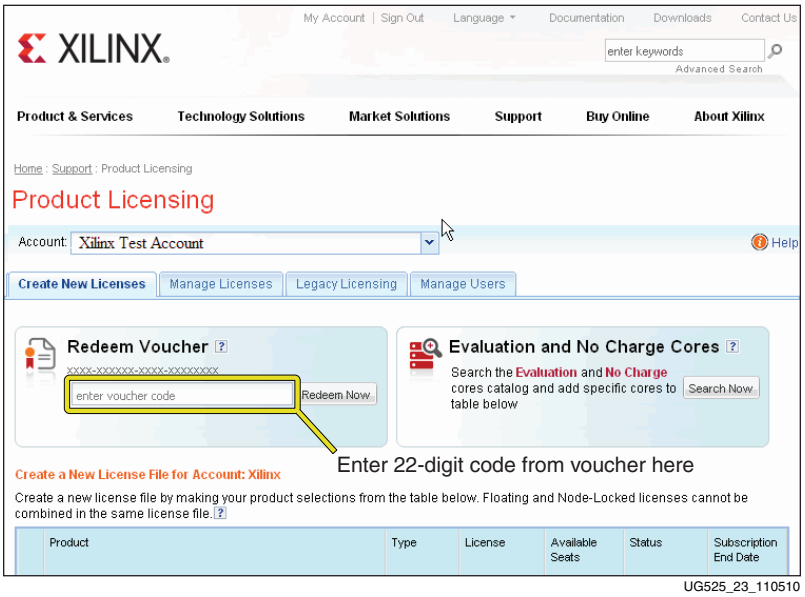


Figure 1-23: **Redeem Voucher**

The software represented by the voucher code is added to the product table and is selected (checked) for licensing, as shown in Figure 1-24.

Note: The software descriptions shown in Figure 1-24 are examples and might differ from the descriptions shown on the actual page.

5. Click **Generate Node Locked License** at the bottom of the page to start the license generation flow (Figure 1-24).

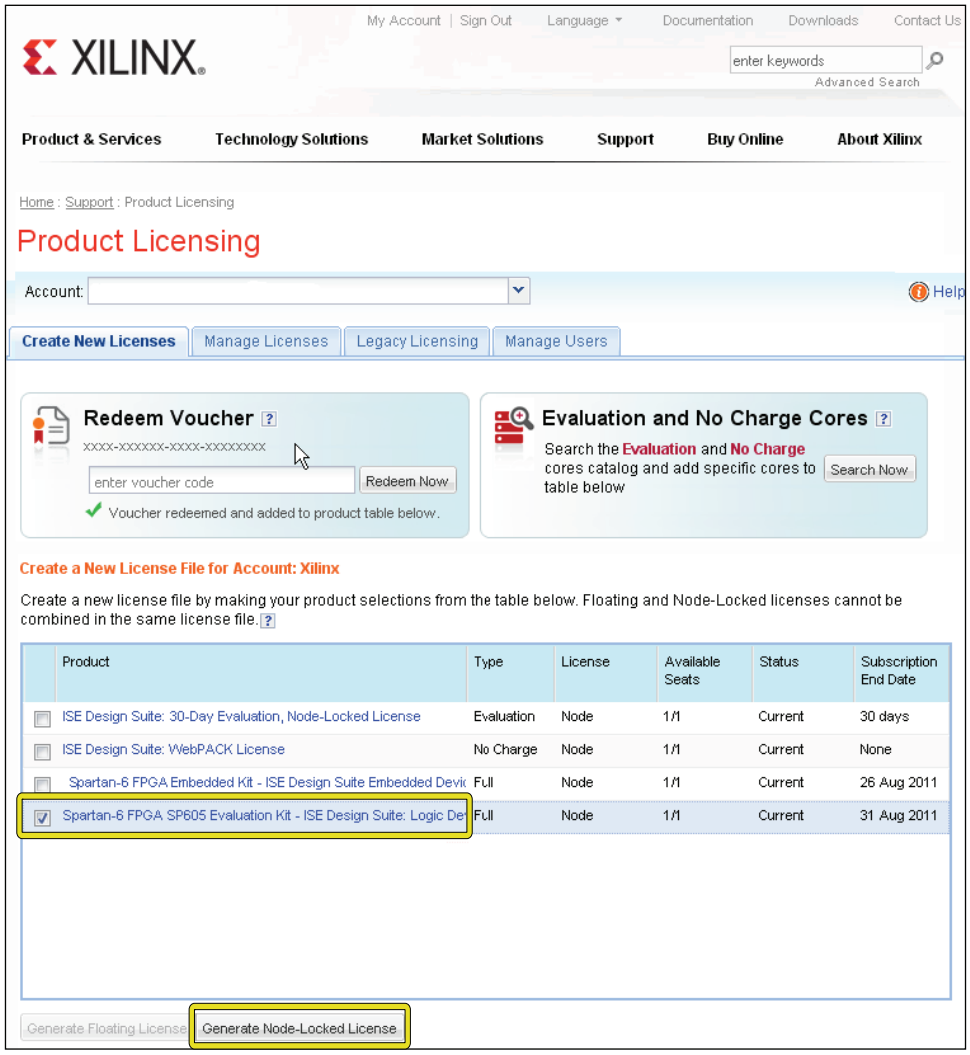
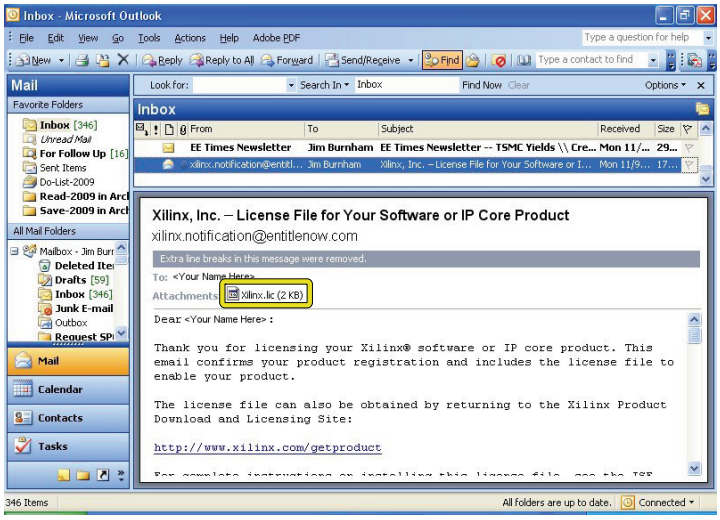


Figure 1-24: **Generate License**

6. When prompted to select a host name for the license, select a host ID. The host ID can be a dongle serial number, Ethernet MAC address, or a disk volume ID.

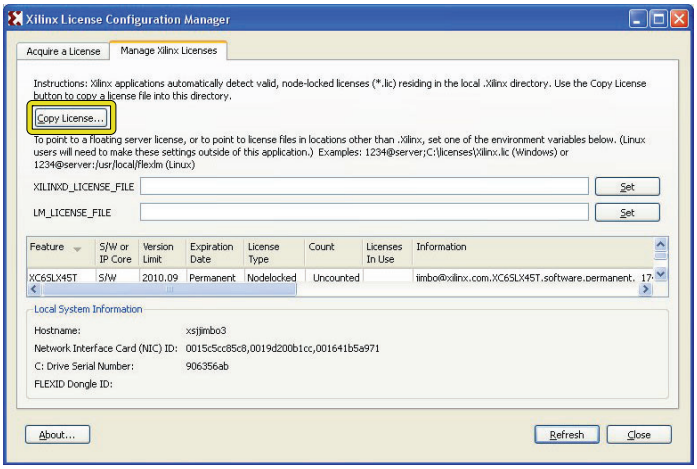
7. When license generation is complete, the license will be emailed. Follow the instructions in the Xilinx License email to complete the licensing process (Figure 1-25).



UG525_25_1105810

Figure 1-25: **Xilinx License Notification E-mail**

8. Go back to the Xilinx License Configuration Manager dialog and click **Copy License...** (Figure 1-26).



UG525_36_110510

Figure 1-26: **Manage Xilinx License Tab**

9. Navigate to the location where the `Xilinx.lic` file is saved and select it (Figure 1-27).

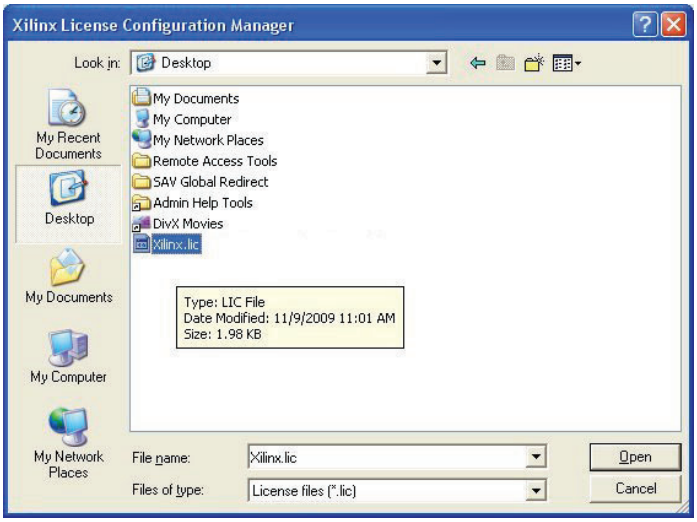


Figure 1-27: **Select the `Xilinx.lic` file**

The ISE software license is now installed. Click **OK** on the Success Dialog (Figure 1-28) to close the Xilinx License Configuration Manager.

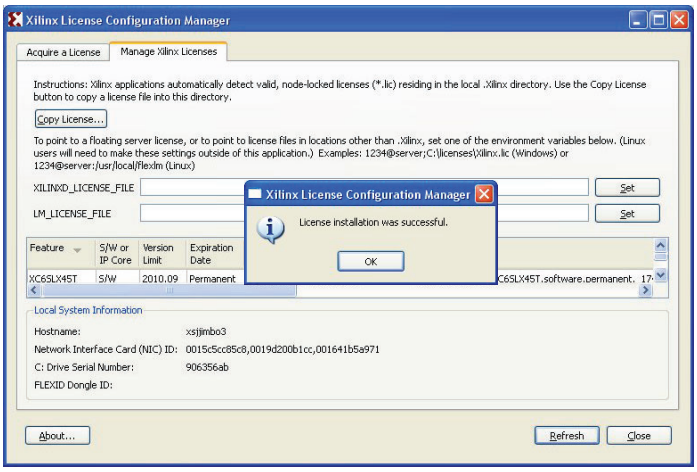


Figure 1-28: **License Installation Successful**

Getting Additional Help and Support

For questions regarding products within the Product Entitlement Account or if it is believed a notification was received in error, send an e-mail message to the appropriate regional Customer Service Representative:

Canada, USA and South America — isscs_cases@xilinx.com

Europe, Middle East, and Africa — eucases@xilinx.com

Asia Pacific including Japan — apaccase@xilinx.com

For technical support including the installation and use of the product license file, contact Xilinx Online Technical Support at www.support.xilinx.com. The following resources for assistance can be found at this site:

Software, IP and Documentation Updates

Access to Technical Support Web Tools

Searchable Answer Database with Over 4,000 Solutions

User Forums

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Appendix A

References

This appendix lists support and document references for Spartan-6 devices and the SP605 Evaluation Kit.

Support Resources

The SP605 Evaluation Kit product website describes the evaluation kit, provides ordering information, and links to other relevant webpages:

- http://www.xilinx.com/products/devkits/EK-S6-SP605-G.htm

The SP605 documentation website provides access to documents, reference design files, and other SP605 board collateral:

- http://www.xilinx.com/products/boards/sp605/reference_designs.htm

The Xilinx support website provides access to a variety of support resources including an answers database search, WebCase support, and contact information:

- http://www.xilinx.com/support

Spartan-6 FPGA Documents

Spartan-6 device documentation is listed here:

DS160, *Spartan-6 Family Overview*
This document outlines the features and product selection of the Spartan-6 family.

DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*
This data sheet contains the DC and switching characteristic specifications for the Spartan-6 family.

UG385, *Spartan-6 FPGA Packaging and Pinouts Specification*
This specification lists device/package combinations, pin definitions, pinout tables, pinout diagrams, thermal specifications and mechanical drawings.

UG380, *Spartan-6 FPGA Configuration User Guide*
This user guide describes configuration interfaces, multi-bitstream management, bitstream encryption, boundary-scan and JTAG configuration, and reconfiguration techniques.

UG381, *Spartan-6 FPGA SelectIO Resources User Guide*
This guide describes the SelectIO™ resources available in all Spartan-6 devices.

UG382, *Spartan-6 FPGA Clocking Resources User Guide*
This user guide describes the clocking resources available in all Spartan-6 devices, including the DCMs and PLLs.

UG388, *Spartan-6 FPGA Memory Controller User Guide*
This user guide describes the Spartan-6 FPGA memory controller block, a dedicated embedded multi-port memory controller that greatly simplifies interfacing Spartan-6 FPGAs using popular memory standards.

UG383, *Spartan-6 FPGA Block RAM Resources User Guide*
This user guide describes the Spartan-6 device block RAM capabilities.

UG384, *Spartan-6 FPGA Configurable Logic Block User Guide*
This user guide describes the capabilities of the configurable logic blocks (CLBs) available in all Spartan-6 FPGAs.

UG386, *Spartan-6 FPGA GTP Transceivers User Guide*
This user guide describes the GTP transceivers available in the Spartan-6 LXT FPGAs.

UG389, *Spartan-6 FPGA DSP48A1 Slice User Guide*
This user guide describes the architecture of the DSP48A1 slice in Spartan-6 FPGAs and provides configuration examples.

UG393, *Spartan-6 FPGA PCB Design and Pin Planning Guide*
This guide provides information on PCB design for Spartan-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

UG654, *Spartan-6 FPGA Integrated Endpoint Block for PCI Express User Guide*
This User Guide describes the function and operation of the Spartan-6 FPGA Integrated Endpoint Block for PCI Express®, including how to design, customize, and implement it.

UG672, *Spartan-6 FPGA Power Management User Guide*
This user guide provides information on the various hardware methods of power management in Spartan-6 FPGAs, primarily focusing on the suspend mode.

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